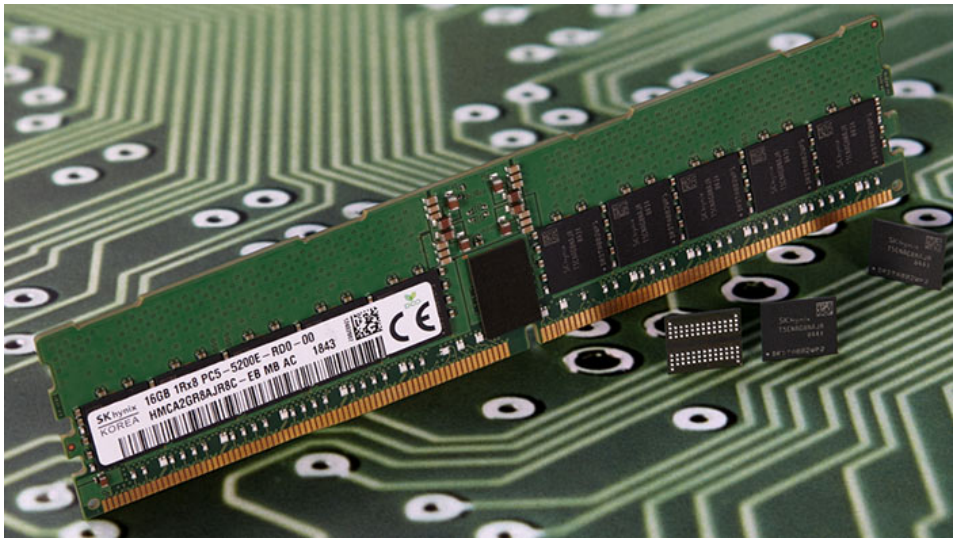
SK Hynix publishes a technical blog about the features of DDR5, a memory standard the company says will be available "in the near future" as it plans to start mass-production sometime "this year."



The company first detailed its DDR5 plan s back in February 2019 with the presentation of a DDR5-6400 memory chip at the International Solid State Circuits Conference. The technology offers two times the bandwidth compared to DDR4, with the aim of reaching over 4800Mbps, allowing it to handle the demands of massively multi-core CPUs.

DDR5 adopts a 32-bank structure based on 8 bank groups, twice as many as the 16-bank structure of DDR4 using 4 bank groups. The burst length (BL) is also up from the 8 of DDR4 to 16, while a Same Bank Refresh function allows the system to access other banks when certain banks are operating, further improving memory access availability. A Decision Feedback Equalisation (DFE) circuit eliminates reflective noise. Further improving reliability are on-die error correction code (ECC) and error check and scrub (ECS).

While the first DDR5 chip from SK Hynix was the aforementioned DDR5-6400 DRAM, the company plans to develop memory up to DDR5-8400. The memory runs at an operating voltage of 1.1V, a -9% reduction from the operating voltage of DDR4, and SK Hynix aims to further reduce power consumption per bandwidth by over -20% over DDR4.

According to IDC, DDR5 is set to account for 22% of the total DRAM market in 2021, before

growing to 43% in 2022.

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