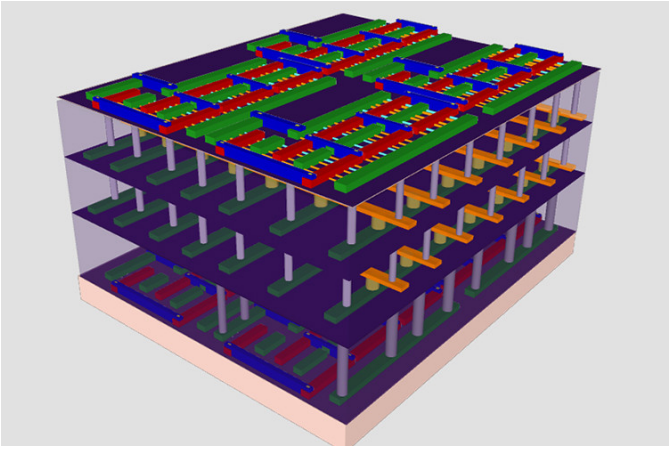
Stanford University researchers present the "skyscraper" chip-- essentially a multilayered take on processor building, with layers of logic atop layers of memory, with thousands of nanoscale "elevators" linking layers.



According to the researchers, such chips are faster and use less electricity than their traditional equivalents, as the architecture avoids the bottleneck-prone wires connecting single-story logic and memory chips. So far a 4-layer chip has been built, but the researchers say the technology can be scalable to higher numbers.

The chips leverage on 3 breakthroughs-- carbon nanotube transistors (CNTs), resistive random access memory (RRAM) and the actual technique behind building layers of logic and memory. The CNTs provide the logic and link the layers of the high-rise chips, while RRAM, being non-silicon based, reduces power requirements.

The production of CNT and RRAM involves a low-heat process, allowing the fabrication of memory layers directly on top of the CNT logic layers. And since such production was achieved in an academic lab, it should be easy enough to replicate in more sophisticated commercial fabrication plants.

"Paradigm shift is an overused concept, but here it is appropriate," researcher H.S. Philip Wong says. "With this new architecture, electronics manufacturers could put the power of a supercomputer in your hand."

Go [Stanford Team Combines Logic, Memory to Build "High-Rise" Chip]